ATOM

Half Length Multimedia PC

User Manual

ATOM

User Manual

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COMPANY PROFILE

Blue Chip Technology is a leading specialist PC product manufacturer in Europe.

Blue Chip Technology provides innovation with quality design and manufacturing from a single source.

Based in the North West of England, our purpose built complex contains both advanced research and development facilities, and manufacturing facilities.

Specialising in the provision of industrial computing and electronic solutions for a wide range of UK and European organisations, Blue Chip Technology has one of the UK's largest portfolios of industrial PCs, peripherals and data acquisition cards. This extensive range of products, coupled with our experience and expertise, enables Blue Chip Technology to offer an industrial processing solution for any application. The ATOM Single Board PC is the latest addition to our portfolio, providing a cost effective product development and volume production tool for OEMs.

A unique customisation and specialised system integration service is also available, delivering innovative solutions to customers problems. The company's success and reputation in this area has led to a number of large design and manufacturing projects for companies such as GEC Marconi, Aston Martin, Shell and British Gas.

British Standards Institute approval (BS EN 9001) means that all of Blue Chip Technology's design and manufacturing procedures are strictly controlled, ensuring the highest levels of quality, reliability and performance.

Blue Chip Technology are also committed to the single European market and continue to invest in the latest technology and skills to provide high performance computer and electronic solutions for a world-wide customer base.

INTRODUCTION

MANUAL OBJECTIVES

This manual describes in detail the Blue Chip Technology ATOM Single Board processor card.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of the ATOM.

The manual is sectioned and includes a User Guide which will help the non technical user to get the unit up and running. A Troubleshooting Guide is also included to help when things go wrong.

We strongly recommend that you study this manual carefully before attempting to interface with ATOM or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Technical Services department with the relevant details.

LIMITATIONS OF LIABILITY

In no event shall Blue Chip Technology be held liable for any loss, expenses or damages of any kind whatsoever, whether direct, indirect, incidental or consequential, arising from the design or use of this product or the support materials supplied with this product. If this product proves to be defective, Blue Chip Technology is only obliged to replace or refund the purchase price at Blue Chip Technology's discretion according to their Terms and Conditions of Sale.

PRECAUTIONS

It is imperative that precautions are taken to avoid Electro-static discharges, or any maltreatment of the on-board battery.

ELECTRO-STATIC DISCHARGES

The devices on this card can be totally destroyed by static electricity. Ensure that you take necessary static precautions, ideally wear an approved wrist strap or touch a suitable ground to discharge any static build up. This should be repeated if the handling is for any length of time.

When carrying the board around, please place it into the anti-static bag in which it came. This will prevent any static electricity build up.

ON-BOARD BATTERY

This board is fitted with a Lithium battery. Great care should be taken with this type of battery. Under NO circumstances should :

- the outputs be shorted
- be exposed to temperatures in excess of 100°C
- be burnt
- be immersed in water

- be unsoldered
- be recharged
- be disassembled

If the battery is mistreated in any way there is a very real possibility of fire, explosion, and harm.

RELATED PUBLICATIONS

The following publications will provide useful information related to the Standard Personal Computer and can be used in conjunction with this manual.

- IBM Personal Computer AT Technical Reference, 1502494, IBM, 1984.
- IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference, 15F0306, IBM, 1987.
- The Programmers PC Sourcebook, Microsoft
- The Winn L. Rosch Hardware Bible, Brady

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USER GUIDE

OVERVIEW

The Blue Chip Technology ATOM single board PC sets new standards for integration of the latest advances in processor, memory, and I/O technologies. The ATOM PISA complies with the new PISA standard providing ISA and PCI bus interfaces on a single card. This half card multimedia PC is an ideal platform for the increasing requirements of today's and tomorrow's embedded applications. The ATOM ISA provides continued support for legacy ISA backplanes.

The flexible design will accept processors operating at 100, 133, 166, 200, 233, 266 and 300MHz, including MMX devices. The user may install 256 KB of asynchronous Cache, or 256 KB or 512 KB of Pipeline Burst Cache RAM in the form of a COAST (Cache On A STick) Module. The memory sub-system is designed to support up to 256MB of EDO DRAM (for improved performance) or standard Fast Page DRAM in standard 72-pin SIMM sockets. A socket accommodates the CPU (turned-pin or SZIF).

The ATOM single board PC utilises Intel's Triton 82430HX PCIset to provide increased integration and performance over other single board PC designs. The Triton PCIset contains an integrated PCI Bus Mastering IDE controller with a high performance IDE interface allowing up to two IDE devices (such as hard drives, CD-ROM readers, etc.). The SMC 37C932 Super I/O controller integrates the standard PC I/O functions: floppy interface, two FIFO serial ports, one EPP/ECP capable parallel port, a Real Time Clock, keyboard and mouse (PS/2) controller.

The ATOM also provides for driving up to twenty external ISA (and four PCI expansion slots - PISA version only).

In addition to superior hardware capabilities, a full set of software drivers and utilities are available to allow advanced operating systems such as Windows™ 95 to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Windows™ 95/98 ready Plug and Play, Advanced Power Management (APM) are available for the ATOM.

BOARD LEVEL FEATURES

- SPGA socket supporting 75 - 300 MHz operation
- On-board 3.3 V CPU voltage regulator
- Intel Triton 82430 PCIset chipset:
  - 82439HX Xcelerated Controller (TXC)
  - PIIX3 PCI ISA IDE Accelerator (PIIX3) bridge
- 256KB or 512 KB PipeLine Burst Level 2 cache or 256 KB Asynchronous Level 2 cache using plug-in COAST connector
- Two SIMM sockets providing up to 256MByte of EDO or FPM DRAM
- C&T 69000 PCI CRT/LCD graphics controller with 2 Mbytes or 69030 with 4MB of video memory
- PCI and ISA expansion busses via a PISA connector or ISA only via ISA connector
- SMC 37C932 I/O controller providing:
  - Dual PCI IDE interfaces
  - Dual floppy interface
  - EPP/ECP bi-directional parallel interface
- PCI 100/10 base-T Ethernet controller
- Dual USB ports
- Stereo sound (SoundBlaster™ compatible)
- Dual RS232 serial ports. RS422/485/IRDA port. option on the second serial port.
- Real-time clock with on-board battery
- PS/2 mouse and keyboard connectors

- Plug-in M-Systems Flash modules.
- Drive for up to 20 ISA and 4 PCI cards (PISA version)

CPU

The ATOM single board PC is designed to operate with Pentium-class Processors running at 2.2, 2.8, 2.9 or 3.3 Volts. An on-board voltage regulator circuit provides the required voltage for the processor from the incoming 5 volt power supply.

The Pentium processor maintains full backward compatibility with the 8086, 80286, i386™ and Intel486™ processors. It supports both read and write burst mode bus cycles, and includes separate on-chip code and data caches which employ a write-back policy. Also integrated into the Pentium processor is an advanced numeric co-processor which significantly increases the speed of floating point operations, whilst maintaining backward compatibility with Intel486™ math co-processor and complying to ANSI/IEEE standard 754-1985.

PROCESSOR SOCKET

SZIF: Processor replacement requires the careful use of a flat blade screwdriver. A heatsink and fan will be required for many of the processors. These will make CPU fitting difficult because of their placement, especially if they reduce the mechanical advantage of the screwdriver. The screwdriver can be cranked to overcome this by putting a bend in it at the point it contacts the edge of the CPU. 3.5mm screwdrivers have been found to be ideal.

Insert the CPU carefully observing the missing pin of the polarisation corner (inspect the pins for alignment first). Place the screwdriver all the way into the special aperture in the socket between CPU and large capacitors. Using only the flat of the blade against the CPU, lever the CPU away from the capacitors until a sharp click indicates proper location. Check that the CPU now sits as far towards the memory end of the socket as possible. The edge should rest against the plastic by the extraction screwdriver aperture.

Removal is an identical operation using the aperture on the memory side and levering towards the capacitors, followed by easy lifting out of the socket.

Turned-Pin: Ensure pins are straight before insertion. Take care not to damage adjacent components during extraction.

SECOND LEVEL CACHE

A second level cache using the COAST connector can complement the Pentium processor's internal cache. Pipeline Burst SRAM provides performance similar to expensive Synchronous Burst SRAMs for only a slight cost premium over the slower performing Asynchronous SRAMs. With the Triton chipset, the performance level of Pipeline Burst and Synchronous SRAMs is identical.

SYSTEM MEMORY

The ATOM single board PC provides two 72-pin SIMM sites for memory expansion. The sockets support 1M x 32 (4 MB), 2M x 32 (8 MB), 4M x 32 (16 MB), 8M x 32 (32 MB), 16M x 32 (64 MB) and 32MB x 32 (128 MB) single-sided or double-sided SIMM modules. Minimum memory size is 8 MB and maximum memory size, using two 32MB x 32 SIMM modules, is 256 MB. Memory timing requires 70 ns fast page devices or, for optimum performance, 60nS EDO DRAM. If the memory bus speed is 60 MHz or slower (75MHz, 90MHz, 120MHz, 150MHz or 180MHz Pentium Processor speed), 70ns EDO DRAM may be used. If the memory bus speed is 66 MHz, 60 ns DRAM should be used. Additionally, 36-bit SIMM modules may be used to provide either standard parity operation or the parity circuitry can be used by the HX chipset to provide ECC correction. EDO DRAM is designed to improve DRAM read performance. Both sockets must be occupied with identical SIMM types as the two sockets are arranged in a bank which provides a 64-bit wide data path. There are no jumper settings required for the memory size or type, this is automatically detected by the system BIOS.

BUS EXPANSION SLOTS

The ATOM is designed for use in an embedded application and provides expansion via PISA or ISA edge connectors. The PISA version can plug into a suitable backplane to drive up to 20 ISA bus expansion cards and 4 PCI expansion cards. The ISA version can drive up to 20 ISA bus expansion cards.

ELECTROMAGNETIC COMPATIBILITY

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

ATOM has been assessed operating in a Blue Chip Technology PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. Subject to those conditions, it meets the requirements for an industrial environment (Class A product).

- The board must be installed in a computer system chassis which provides screening suitable for an industrial environment.
- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.
- The board must be installed with the optional back plate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.
- Most EMC problems are caused by the external cabling to boards. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen: they are far superior to those which earth the screen by a simple "pig-tail".
- The keyboard and mouse will play an important part in the compatibility of the processor card since they are ports into the board. Similarly, they will affect the compatibility of the complete system. Fully compatible peripherals must be used otherwise the complete system could be degraded. They may radiate or behave as if keys/buttons are pressed when subject to interference. Under these circumstances it may be beneficial to add a ferrite clamp on the leads as close as possible to the connector. A suitable type is the Chomerics type H8FE-1004-AS.
- Ensure that the screens of any external cables are bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

Warning
This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

SPECIFICATION

ATOM Power Requirement	+5 V ± 5%	Required for processor operation.
	+12 V ± 5%	Required for Network /Audio.
	+3.3 V ± 5%	⎫ Not required for board operation.
	-5 V ± 5%	⎬ The ISA, & PCI voltage
	-12 V ± 5%	⎭ rails are linked on board.

Typical System

Consumption	3.5A 5V 0.15A 12V	K6-2/300, 16 MB RAM, 256 KB cache
	2.0A 5V 0.15A 12V	C6 200, 32MB RAM, 256KB cache IDT C6MP200 3.3V 66MHz bus.
Temperature	Non-Operating Operating (min. airflow of 100 lfm)	-40°C to +70°C +0°C to +55°C
Shock	Non-Operating	Half sine, 2ms, 1 m drop
Vibration	Non-Operating Operating	5 Hz - 500 Hz, 3.1 g RMS random 10 Hz - 500 Hz, 1.0 g RMS random
EMC	Emissions Immunity	EN55022 (A) EN50082-2 in a Blue Chip ICON Industrial PC Chassis
MTBF	Calculated	>100,000 Hrs
Dimensions	Board only	338 x 122 mm {40mm height with COAST – large DRAM or large heatsink may affect this}

Power Consumption figures given are for typical configurations.

This information is preliminary and is provided only as a guide to calculating approximate total system power usage when additional resources are added.

HARDWARE DESCRIPTION

CHIPSET

The Intel 82430HX PCIset consists of the 82439HX Xcelerated Controller (TXC) and one 82371SB PCI/ISA IDE Xcelerator (PIIX3) bridge chip.

82439HX XCELERATED CONTROLLER (TXC)

The 82439HX provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. The TXC also controls access to memory and generates snoop controls to maintain cache coherency. The TXC comes in a 324-pin BGA package and includes the following features:

- Microprocessor interface control
- Integrated L2 write-back cache controller
  - — Pipeline burst SRAM
  - — 256 KB direct-mapped
- Integrated DRAM controller
  - — 64 bit path to memory
  - — Support for EDO and fast page DRAM
  - — Parity and non-parity support
- Fully synchronous PCI bus interface
  - — 25/30/33 MHz bus speed
  - — PCI to DRAM > 100 MB/sec
  - — Up to four PCI masters in addition to the PIIX3

PCI/ISA IDE XCELERATOR (PIIX3)

The PIIX3 provides the interface between the on-board PCI and ISA buses and integrates a dual channel fast IDE interface capable of supporting two devices. The PIIX3 integrates seven DMA channels, one 16-bit timer/counter, two eight-channel interrupt controllers, PCI-to-AT interrupt mapping circuitry, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry together onto the same device. The PIIX3 comes in a 208-pin QFP package and includes the following features.

- Interface between the PCI and ISA buses
- Universal Serial Bus controller
  - — Host/hub controller
- Integrated fast IDE interface
  - — Support for two devices
  - — PIO Mode 4 transfers up to 16 MB/sec

— Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers

— Bus master mode

- PCI 2.1 compliant
- Enhanced fast DMA controller
- Interrupt controller and steering
- Counters/timers
- SMI interrupt logic and timer with fast on/off mode

UNIVERSAL SERIAL BUS (USB)

The ATOM single board PC features two USB ports available via cable set. The ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. ATOM fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible. Features of the USB include:

- Self-identifying “hot pluggable” peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol

NOTE

Computer systems that have an unshielded cable attached to the USB port might not meet FCC Class B requirements, even if no device or a low speed (sub-channel) USB device is attached to the cable. Use shielded cable that meets the requirements for high speed (fully rated) devices.

I/O CONTROLLER

IDE SUPPORT

The ATOM single board PC provides one high performance bus-mastering PCI IDE interface capable of supporting PIO Mode 3 and Mode 4 devices. The system BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes as well as AT API (e.g. CD-ROM) devices on the IDE interface. Detection of IDE device transfer rate and translation mode capability is automatically determined by the system BIOS.

In the Windows™ 95/98 environment, a driver can allow the IDE interface to operate as a PCI bus master capable of supporting PIO Mode 4 devices with transfer rates up to 16MB/sec while minimising the system demands upon the processor. Normally, programmed I/O operations require a substantial amount of CPU bandwidth. In true multi-tasking operating systems like Windows™ 95/98, the CPU bandwidth freed up by using bus mastering IDE can be used to complete other tasks while disk transfers are occurring.

Microsoft will provide this driver for Windows™ 95/98, other software vendors may make drivers

available for other operating systems.

Detailed information on the PCIset is available in the Intel 82430 PCIset data sheet.

SMC 37C932 SUPER I/O CONTROLLER

Control for the integrated serial ports, parallel port, floppy drive, RTC and keyboard controller is incorporated into a single component, the SMC 37C932. This component provides:

- Two powered NS16C550-compatible UARTs with send/receive 16 byte FIFO
- Multi-mode bi-directional parallel port
  - Standard mode; IBM and Centronics compatible
  - Enhanced Parallel Port (EPP) with BIOS/Driver support
  - High Speed mode; Extended Capabilities Port (ECP) compatible
- Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)
- Integrated Real Time Clock
- Integrated 8042 compatible keyboard/mouse controller

The 37C932 is normally configured by the BIOS automatically, however configuration of these interfaces is possible via the CMOS set-up program that can be invoked during boot-up. The serial ports can be enabled as various standard COM ports, or disabled. The parallel port can be configured as normal, bi-directional, EPP/ECP, or disabled. The floppy interface is also configurable.

Header connectors located near the top of the board allow cabling to use these interfaces. Take care to observe the polarity of the headers. Pin 1 is placed at the metal bracket end of the board on all the open headers.

FLOPPY CONTROLLER

The 37C932 is software compatible with the DP8473 and 82077 floppy disk controllers.

The floppy interface can be configured for 360 KB or 1.2 MB 5¼" media or for 720 KB, 1.44 MB, or 2.88 MB 3½" media in the BIOS set-up. By default, the Floppy A interface is configured for 1.44 MB and Floppy B is disabled.

KEYBOARD/MOUSE INTERFACE

A PS/2 keyboard/mouse connector is located on the back panel side of the single board PC. A splitter cable allows mouse and keyboard connection, else only the keyboard occupies this connector. The mouse interface is also available through a polarised header. A Polyswitch resetable fuse protects the 5V lines to these connectors. Care must be taken to turn off the system power before installing or removing a keyboard or mouse, otherwise the fuse may trip. The Polyswitch will reset itself once the fault condition is cleared and the power to the circuit is removed, allowing it to cool.

The integrated 8042 microcontroller contains the AMI Megakey keyboard/mouse controller code which, besides providing traditional keyboard and mouse control functions, supports Power-On/Reset (POR) password protection. The POR password can be defined by the user in the Setup program. The keyboard controller also provides the facility for a <CTRL><ALT><DEL> "hot key" sequence to perform a system software reset. It performs this by jumping to the beginning of the BIOS code and running the POST operation.

REAL TIME CLOCK, CMOS RAM AND BATTERY

The integrated Real Time Clock (RTC) is DS1287 and MC146818 compatible and provides a time of day clock, 100-year calendar with alarm features. The RTC can be set via the BIOS SETUP program. The RTC also supports 242 bytes of battery-backed CMOS RAM in two banks which is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SET-UP program. Also, the CMOS RAM values can be cleared to the system defaults by using a configuration jumper on the single board PC. The appendix lists the jumper configurations.

An on-board Lithium battery provides power to the RTC and CMOS memory. The battery has an estimated lifetime of three years if the board remains unpowered. When the system is powered up, power is drawn from the power supply to extend the life of the battery.

ATOM is Year 2000 compliant

GRAPHICS SUBSYSTEM

The ATOM single board PC is provided with the very latest C&T 69000 or 69030 graphics controller with 2 or 4 MB of graphics memory respectively. Both CRT and LCD interfaces are provided. ATOM supports a wide variety of monochrome and colour Single-Panel, Single-Drive (SS) and Dual-Panel, Dual Drive (DD) passive STN and active matrix TFT/MIM LCD, EL and plasma panels. ATOM supports a wide range of panel resolutions.

The 69000 and 69030 have a 32-bit graphics engine that provides acceleration for scaling the video display without compromising picture quality or frame rate. Hardware acceleration for graphics functions such as line draws, System-to-screen and screen-to-screen BitBLTs, ROPs, which optimise performance operation under Windows™ and other GUI environments.

Note that Chips and Technology products, previously a part of Intel Corporation, are now manufactured by Asiliant Technologies.

DISPLAY CAPABILITIES

The 2MB of video memory can support a variety of resolutions.

The representation of each picture element (pixel) is key to working out capability.

256 colours requires 8 bits (1byte), 64K colours 16 bits (2bytes), 16M colours 24 bits (3bytes).

So 640x480x16M colours requires 640x480x3 bytes = 921600; easily fits into our 2,097,152 bytes of memory.

The drivers supplied from C&T also need to support the desired resolution. These generally support 640x480x16M, 800x600x16M, 1024x768x64K, 1280x1024x256 and 1600x1200x256. However, 16:9 format plasma panel and portrait mode have been provided previously.

The 69030's 4MB of video memory allows higher resolutions/colour depth or independent CRT/panel displays. Resolutions available are up to 1280x1024x16M and 1600x1200x64K in single display mode.

Be aware that driving older or cheaper monitors beyond their capabilities can destroy them. LCD panels can also be easily damaged!

Later BIOSs allow panel choice to be made in setup. This was previously achieved by flash update.

BIOS

The ATOM single board PC uses a Phoenix BIOS and a C&T Video BIOS both of which are stored in EPROM/Flash. In addition to the System and Video BIOSs, the EPROM also contains the Setup utility, Power-On Self Tests (POST), and the PCI auto-configuration utility. This single board PC supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a revision code.

SYSTEM SETUP UTILITY

The ROM-based Setup utility allows the configuration to be modified without opening the system for most basic changes. The Setup utility is accessible only during the Power-On Self Test (POST) by pressing the <F2> key after the POST memory test has started and before boot begins. A prompt may be enabled that informs users to press the <F2> key to access Setup. Deep power-down displays may not light up in time

to display this message. See the BIOS user manual for further details.

CONNECTING AN LCD TO ATOM

Unfortunately, connecting an LCD panel to a PC is not as simple as it is for a CRT. At the time of writing this manual there is still no universally accepted standard interface for LCDs. We strongly recommend that if you are in any doubt about connecting a LCD panel to ATOM you contact our Technical Services team with full details of the target display. **ALWAYS** check your wiring/voltage setting ***before*** you switch on.

JUMPERS

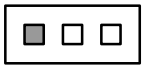
Very few jumpers are used on the board to select various options. Most of the configuration is achieved through software set-up. Some of the jumpers are factory set to suit particular semiconductor options. These must not be disturbed, or damage to the board may ensue.

Table of Jumpers

JUMPER	AREA OF INFLUENCE	LINK	ACTION
J1	CMOS Battery Support	None CLR NORM	Not Allowed Clear CMOS RAM Use on-board battery
JP6	CPU and PCI bus speed plus CPU internal speed		See Jumper Section
J21	Panel voltage supply	3V/5V	3.3V supply 5V supply

CMOS BATTERY SOURCE (CLEAR CMOS) J1

CMOS Clear **J1**
Normal Clear



This jumper is used to clear the CMOS RAM in the event that the contents become corrupt. It selects the source of backup power to the CMOS RAM, and also allows the CMOS to be cleared down to the default settings.

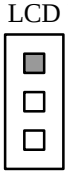
Fitting the link to the "CLR" position with the power off, allows on-board capacitors to discharge and will reset the CMOS memory. The jumper should then be returned to the "NORM" position to restore normal operation.

PANEL POWER SUPPLY J21

This sets the power supplied to the panel interface to 5V or 3.3V.

■ = Pin 1

LCD Panel Supply **J21**



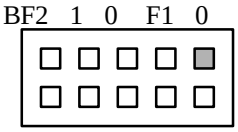
J1/J21: Link two pins as appropriate **without** power applied. Orientations as in diagrams of board outline p**Error! Bookmark not defined.**. BUS Connectors

CPU SPEED SETTING JP6

This set of jumpers is provided to set the CPU internal speed and the CPU external bus speed.

The external bus speed is always as shown in the tables in this document.

Unfortunately the CPU manufacturers do not have any consistency of settings for particular multiplication settings - each CPU type requires information from the data sheet! Many common, current values have been listed in this document but other requirements can be determined by understanding the BF[2-0] operation: inserting a jumper sets the signal to logical low (0V).



Pin 1
0 = Jumper present
1 = Jumper absent

Host Bus Speeds available (JP) = Jumper Present

F1	F0	Host Bus Speed	PCI Bus Speed
0(JP)	0(JP)	50MHz	25MHz
1	0(JP)	60MHz	30MHz
0(JP)	1	66MHz	33MHz
1	1	Not allowed	-

Common Processor multiplier jumper settings

(JP) = Jumper Present

BF2	BF1	BF0	P	MMX	C6	K6(-2)[0:7]	K6(-2)[F:8]
0(JP)	0(JP)	0(JP)			-	4.5	4.5
0(JP)	0(JP)	1			5	5	5
0(JP)	1	0(JP)			4	4	4
0(JP)	1	1			-	5.5	5.5
1	0(JP)	0(JP)	2.5	2.5	-	2.5	2.5
1	0(JP)	1	3	3	3	3	3
1	1	0(JP)	2	2	2	2	6
1	1	1	1.5	3.5	4	3.5	3.5

The internal CPU speed is expressed as a multiplication of this frequency.
Internal CPU speed from Host Bus Speed

Multiplier	50MHz	60MHz	66MHz
1.5	75	90	100
2	100	120	133
2.5	125	150	166
3	150	180	200
3.5	175	210	233
4	200	240	266
4.5	225	270	300
5	250	300	333
5.5	275	330	366
6	300	360	400

USER-INSTALLABLE UPGRADES

SYSTEM MEMORY

The table shows the possible memory combinations. ATOM will support both Fast Page DRAM or EDO DRAM SIMMs, but they cannot be mixed. Parity/Error Correction is supported when using parity SIMMs (x36).

SIMM requirements are 70ns Fast Page Mode or 60nS EDO DRAM (70 ns EDO may be used with a 60 MHz or slower external CPU clock) with tin-lead connectors.

SIMM 1,2 (BANK A) SIMM TYPE (AMOUNT)	TOTAL SYSTEM MEMORY
1M X 32 (4 MB)	8 MB
2M X 32 (8 MB)	16 MB
4M X 32 (16 MB)	32 MB
8M X 32 (32 MB)	64 MB
16M X 32 (64 MB)	128 MB
32M X 32 (128 MB)	256 MB

Note: SIMMs may be parity (x 36) or non-parity (x 32)

EDO DRAM

Extended Data Out (or Hyper Page) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge, unlike standard fast page mode DRAM which tri-states the memory data when CAS# negates to precharge for the next cycle. With EDO, the CAS# precharge overlaps the data valid time, allowing CAS# to negate earlier while still satisfying the memory data valid window time.

REAL TIME CLOCK BATTERY REPLACEMENT

The on-board battery may be replaced using a Duracell DL2032 3 volt button cell, or equivalent.

GRAPHICS MEMORY OPTION

The C&T B69000 has 2 MB of DRAM installed for graphics. The B69030 has 4MB of memory. These are build options – no upgrade is possible.

SOLID STATE DISK SUPPORT

The ATOM supports the use of M-Systems' DiskOnChip 2000 or DiskOnChip Millennium Flash Modules as solid-state disks. The notes below detail the use of the device with MS-DOS. If support is required for other operating systems, please consult Blue Chip Technology Technical Services, or M-Systems web-site at www.m-sys.com, for drivers and application notes.

The DiskOnChip 2000 and Millennium contain a built-in copy of the M-Systems industry-standard TrueFFS software, which allows the DiskOnChip to operate as a standard disk drive. The DiskOnChip may also contain the operating system thereby permitting systems to boot without a hard disk. The DiskOnChip may also be configured as the boot device in systems with a hard disk (see the section "Configuring the DiskOnChip as the First Drive").

The DiskOnChip is a self-contained device, the installation of which does not necessarily require any software installation. The basic design of the DiskOnChip allows for full upward and downward compatibility by supporting an unlimited capacity. Future DiskOnChip devices with higher densities will be fully compatible with today's capacities of 2 to 288 MBytes, and the standard DiskOnChip socket.

INSTALLING THE DISKONCHIP

Before installing or removing the DiskOnChip, please read the section on Electro-Static Discharges at the beginning of this manual. It is essential that you discharge any static electricity from your body before touching the board or DiskOnChip module. Use the following procedure to install the DiskOnChip:

- Align pin 1 on the DiskOnChip with pin 1 of the socket (adjacent to the battery).
- Push the DiskOnChip into the socket carefully until it is fully seated.
- Check that the DiskOnChip is installed securely, and that there are no bent pins.

Caution: The DiskOnChip may be permanently damaged if installed incorrectly!

To install the DiskOnChip as drive C on a system without a hard disk, set the CMOS setup of drive C to "not installed" (indicating that no physical magnetic disk is installed), and reboot the computer. The DiskOnChip will install as drive C. The DiskOnChip should then be formatted with the System files in order for it to be a bootable drive. See *"Configuring the DiskOnChip as the BOOT device"* below.

To install the DiskOnChip as drive D on a system with a hard disk, reboot the system, and the DiskOnChip will automatically install as drive D.

To install the DiskOnChip as Drive C on a system with a hard disk, see below *"Configuring the DiskOnChip as the First Drive"*.

CONFIGURING THE DISKONCHIP AS THE BOOT DEVICE

To configure the DiskOnChip as the boot device, the operating system files have to be copied to it. Copying the operating system files into DiskOnChip is done in exactly the same way as any other hard disk. The following is an example of a typical initialisation process:

- Set the DiskOnChip as a regular drive in your system (not a boot drive).
- Install a bootable floppy diskette in drive A and boot the system.
- At the DOS prompt, type `SYS C:` to transfer the DOS system files to the DiskOnChip (assuming the DiskOnChip is installed as drive C).
- Copy any files needed into the DiskOnChip.
- Remove the floppy diskette and reboot the system.

The system will boot from the DiskOnChip, and will allow you to run and access any files that have been copied into the DiskOnChip.

CONFIGURING THE DISKONCHIP AS THE FIRST DRIVE

The DiskOnChip can be configured to be installed as the last drive (default), or as the first drive in the system. When configured as the last drive, the DiskOnChip is installed as disk D if there is one other hard drive installed, and as drive C if no other hard disk is installed. When configured as the first drive, the DiskOnChip is always installed as drive C. The DiskOnChip is shipped from the factory, configured to install as the last drive. To configure the DiskOnChip to be installed as the first drive, proceed as follows:

- Boot the system and make sure the DiskOnChip is installed correctly as drive D
- At the DOS prompt type: `DUPDATE D: /FIRST /S:DOC123.EXB`

After re-booting the system, the DiskOnChip will appear as drive C:

USING THE ADDITIONAL IO FUNCTIONS

WATCHDOG TIMER OPERATION

The ATOM includes a watchdog timer circuit, which may be used to monitor software or processor hardware failure. The time-out period of the watchdog is fixed at 500 milliseconds. It may be enabled or disabled by using the software interrupt at INT 50h.

Note that the watchdog is disabled following a power on or a reset sequence.

The following code demonstrates the control of the watchdog timer.

Enable/Disable Watchdog

Use the software interrupt as follows:

Calling Registers:	AH = 05 AL = 01 to enable, 00 to disable
Perform INT 50h.	
Return Registers:	AH = 00 (success) or FF (failure), and Carry Flag is clear if successful, set if unsuccessful

Refresh Watchdog

Use the software interrupt as follows at least once every 500 milliseconds:

Calling Registers:	AH = 06
Perform INT 50h.	
Return Registers:	None

ADDRESS MAPS

I/O MAP

The following table lists the I/O addresses used by single board PC devices. Some of these devices may not be present in all configurations. Some devices (serial ports, parallel ports etc.) may be configured for various addresses or disabled. These I/O locations are listed in the Variable Resources column.

ADDRESS (HEX)	SIZE Bytes	FIXED RESOURCES	VARIABLE RESOURCES
0000 - 000F	16	PIIIX - DMA 1	
0020 - 0021	2	PIIIX - Interrupt Controller 1	
002E - 002F	2	Ultra I/O configuration registers	
0040 - 0043	4	PIIIX - Timer 1	
0060	1	Keyboard Controller Data Byte	
0061	1	PIIIX - NMI, speaker control	
0064	1	Kbd Controller, CMD/STAT Byte	
0070, bit 7	1 bit	PIIIX - Enable NMI	
0070, bits 6:0	7 bits	RTC, Address	
0071	1	RTC, Data	
0080 - 008F	16	PIIIX - DMA Page Register	
00A0 - 00A1	2	PIIIX - Interrupt Controller 2	
00B2 - 00B3	2	PIIIX - APM Control / Status	
		Interrupt Controller 2	
00C0 - 00DE	31	PIIIX - DMA 2	
00F0	1	Reset Numeric Error	
0100 - 0107	8	Reserved for Board Confign.	
0170 - 0177	8		
01F0 - 01F7	8		Primary IDE Channel
0200 - 0207	8		Gameport Joystick
0220			Audio
0278 - 027B	4		
02E8 - 02EF	8		
02F8 - 02FF	8		Serial Port 2
0376-377	2		
0378 - 037F	8		Parallel Port 1
0388			Audio
03B0 - 03BB	4		C&T69000/69030
03BC - 03BF	4		
03C0 - 03DF	16		C&T69000/69030
03E8 - 03EF	8		
03F0 - 03F5	6		Floppy Channel 1
03F6	1		Pri IDE Chan Cmnd Port
03F7 (Write)	1		Floppy Chan 1 Cmnd
03F7, bit 7	1 bit		Floppy Disk Chg Chan 1
03F7, bits 6:0	7 bits		Pri IDE Chan Status Port
03F8 - 03FF	8		Serial Port 1
LPT + 400h	3		ECP regs, LPT base + 400h
04D0 - 04D1	2	Edge/Level INTR Control Reg.	
0CF8 - 0CFC*	4	PCI Config Address Reg.	
0CF9	1	Turbo & Reset control Reg.	
0CFC - 0CFF	4	PCI Config Data Reg	
FFA0 - FFA7	8		1ary Bus Master IDE regs
FFA8 - FFAF	8		2ary Bus Master IDE regs
FF00-FF07	8		IDE Bus Master Reg.

*only accessible by DWORD accesses.

MEMORY MAP

ADDRESS RANGE (DECIMAL)	ADDRESS RANGE (HEX)	SIZE	DESCRIPTION
1024K - 131072K	100000 - 8000000	127M	Extended Memory
896K - 1023K	E0000 - FFFFF	128K	Phoenix System BIOS (not available for UMB)
824K - 832K	CE000 - CFFFF	8K	Solid State Disk Pages
848K - 879K	D4000 - DBFFF	32K	BIOS Extensions
800K - 823K	C8000 - CDFFF	23K	Available HI DOS memory (open to ISA and PCI bus)
640K - 799K	A0000 - C7FFF or CAFFF	160K	On-board video memory and BIOS (32/44K BIOS)
639K	9FC00 - 9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K - 638K	80000 - 9FBFF	127K	Extended conventional
0K - 511K	00000 - 7FFFF	512K	Conventional

PCI CONFIGURATION SPACE MAP

The Triton chipset uses Configuration Mechanism 1 to access the PCI configuration space. The PCI Configuration Address register is a 32-bit I/O register located at 0CF8h, the PCI Configuration Data register is a 32-bit I/O register located at 0CFCh. The PCI Configuration Address register is only accessible by a DWORD access, the PCI Configuration Data register is accessible by DWORD, WORD or BYTE accesses.

ACCESS TO I/O CONFIGURATION SPACE USING MECHANISM #1

Using a DWORD write command, output the required I/O configuration address to I/O port CF8H

1. Using a DWORD read or write command, read or write data from the I/O port CFCH

NOTE: Any address output to CF8H is always on a 4 byte (DWORD) boundary. You can read or write any BYTE, WORD or DWORD in the four byte range by using the correct offset as follows:

DWORD @ CFCh

WORD @ CFCh or CFEh

BYTE @ CFCh, CFDh, CFEh or CFFh

CONFIGURATION ADDRESS REGISTER BIT DEFINITION

BIT	FUNCTION / SETTING
31	1
30 - 24	RESERVED
23 -16	BUS NUMBER
15 - 11	DEVICE NUMBER
10 - 8	FUNCTION NUMBER
7 - 2	REGISTER NUMBER
1	0
0	0

CONFIG SPACE ENABLE FLAG (Bit 31): Always 1 to indicate I/O access is to configuration space.

RESERVED (Bits 30-24): Always 00h

BUS NUMBER (Bits 23-16): Always 00h unless a bridge card is installed in a PCI slot

DEVICE NUMBER (Bits 15-11): Used to indicate a specific PCI device. The Triton TSC has a

predefined device number of 00000h. The PIIIX and four PCI slots also have specific device numbers, that device number is determined by which PCI Address/Data line is connected to the device's ID SEL pin. Specific mapping information is detailed in the table below.

FUNCTION NUMBER (Bits 10-8): Used to indicate a specific function in multifunction PCI devices. The PIIIX is the only multi-function device on ATOM located on the single board PC. Use 00h for the basic PIIIX device and 01h for the PCI IDE BUS MASTER FUNCTION. For a multi-function PCI add-in card, refer to the card's documentation to determine the allowable function numbers.

REGISTER NUMBER (Bits 7-2): Defines one of 64 DWORD locations for a specific PCI device.

Note that Bits 1 and 0 must always be 0h for DWORD access.

The table below lists the PCI bus and device numbers used by the single board PC. It also lists the data range that must be written to the I/O Configuration Address register to access the device.

DEVICE	BUS/DEVICE/ FUNCTION	ID SEL	I/O CONFIG ADDRESS REGISTER
TSC	00 / 00 / 0	N/A	8000 0000 - 8000 00FC
PIIIX	00 / 07 / 0	AD18	8000 3800 - 8000 38FC
PIIIX-IDE BUS MASTER	00 / 07 / 1	AD18	8000 3900 - 8000 39FC
PIIX-Serial Bus Controller (USB)	00 / 07 / 2	AD18	8000 3A00 - 8000 3AFC
C&T69000/69030	00 / 08 / 0	AD13	8000 4000 - 8000 40FC
RTL8139 (Ethernet)	00 / 09 / 0	AD14	8000 4100 - 8000 41FC
Slot 1		AD19	
Slot 2		AD20	
Slot 3		AD21	
Slot 4		AD22	

INTERRUPTS & DMA CHANNELS

The following tables list the Interrupt and DMA Channel configuration options for on-board devices. The serial ports, parallel ports, and IDE controller can be configured using SETUP, or any other Plug and Play resource manager (such as the Windows™ 95/98 Device Manager). The Graphics interrupt is assigned by the auto-configure utility during boot up.

IRQ	RESERVED INTERRUPTS
NMI	I/O Channel Check
0	Interval Timer
1	Keyboard buffer full
2	Cascade interrupt from slave PIC
3	Serial 2 (COM2)
4	Serial 1 (COM1)
5	Audio
6	Floppy Controller
7	Parallel (LPT1)
8	Real time clock
9	VGA if used, USB
10	
11	Ethernet
12	PS/2 Mouse (if present)
13	Math co-processor
14	Primary E-IDE
15	

DMA	RESERVED
0	Audio*
1	Audio*
2	Floppy
3	
4	Cascade channel
5	
6	
7	

* Reconfigurable

CONNECTORS

BACK PANEL CONNECTORS

The back panel houses the following connectors:

*VIDEO CONNECTOR **P18** (15 WAY CONDENSED D-TYPE)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Analogue RED	2	Analogue GREEN
3	Analogue BLUE	4	Not Used
5	0 Volts (Ground)	6	0 Volts (Ground)
7	0 Volts (Ground)	8	0 Volts (Ground)
9	5V limited current	10	0 Volts (Ground)
11	Not Used	12	DCD
13	Horizontal Sync	14	Vertical Sync
15	DCC		

PS/2 KEYBOARD PORT P19 (6 WAY MINI-DIN)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Keyboard Data	2	Mouse Data
3	Ground	4	+5 Volts (fused)
5	Keyboard Clock	6	Mouse Clock

*RS232 SERIAL PORT 1 **P20** (9 WAY D-TYPE)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Data Carrier Detect	2	-Receive Data
3	-Transmit Data	4	-Data Terminal Ready
5	Ground	6	-Data Set Ready
7	-Ready To Send	8	-Clear To Send
9	-RI		

*ETHERNET UTP CONNECTOR **P25** (8 WAY RJ45)*

PIN N°	SIGNAL
1	+VE TRANSMIT
2	-VE TRANSMIT
3	+VE RECEIVE
4	NC
5	NC
6	-VE RECEIVE
7	NC
8	NC

INTERNAL I/O HEADERS & CONNECTORS

The board has a number of internal peripheral connections:

*PRIMARY E-IDE CONNECTOR **P13** (2X20 WAY HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	-Reset	2	Ground
3	Data bit 7 (HD)	4	Data bit 8 (HD)
5	Data bit 6 (HD)	6	Data bit 9 (HD)
7	Data bit 5 (HD)	8	Data bit 10 (HD)
9	Data bit 4 (HD)	10	Data bit 11 (HD)
11	Data bit 3 (HD)	12	Data bit 12 (HD)
13	Data bit 2 (HD)	14	Data bit 13 (HD)
15	Data bit 1 (HD)	16	Data bit 14 (HD)
17	Data bit 0 (HD)	18	Data bit 15 (HD)
19	Ground	20	Polarisation
21	Drive Request	22	Ground
23	-IO Write (HD)	24	Ground
25	-IO Read (HD)	26	Ground
27	Drive Ready	28	Cable select 330ohm to 0V
29	Drive Acknowledge	30	Ground
31	IRQ14	32	Not Used
33	Address 1 (HD)	34	1K ohm to 0V
35	Address 0 (HD)	36	Address 2 (HD)
37	-Chip Select 0 (HD)	38	-Chip Select 1 (HD)
39	IDE LED Drive	40	Ground

*ECP/EPP PARALLEL PORT **JP1** (2X13 WAY HEADER)*

PIN N°	SIGNAL	PIN N°	SIGNAL
1	-Strobe	2	-Auto Feed XT
3	Data bit 0	4	-Error
5	Data bit 1	6	-Initialise
7	Data bit 2	8	-Select (input)
9	Data bit 3	10	Ground
11	Data bit 4	12	Ground
13	Data bit 5	14	Ground
15	Data bit 6	16	Ground
17	Data bit 7	18	Ground
19	-Acknowledge	20	Ground
21	Busy	22	Ground
23	Paper Empty	24	Ground
25	Select (Output)	26	Polarisation

*PS/2 MOUSE PORT **JP2** (5 WAY HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Mouse Data	2	Polarisation
3	Ground	4	+5 Volts (fused)
5	Mouse Clock		

*RS232 SERIAL PORT 2 **P21** (2X5 WAY HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	-Data Carrier Detect	2	-Receive Data
3	-Transmit Data	4	-Data Terminal Ready
5	Ground	6	-Data Set Ready
7	-Ready To Send	8	-Clear To Send
9	-RI	10	Polarisation

*DUAL USB PORTS **JP3** (2X5 WAY HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	USB VCC0	2	Ground
3	USB DATA0-	4	USB Ground1
5	USB DATA0+	6	DATA1+
7	USB Ground0	8	DATA1-
9	Ground	10	USB VCC1

*LCD PRIMARY CONNECTOR **P11** (2X25 WAY 2MM HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	3.3v or 5v as selected	2	Vertical Sync
3	Switched +12 volts	4	Ground
5	Switched VEE	6	Horizontal Sync
7	Switched +5 volts	8	Ground
9	Switched +5 volts	10	General Purpose 1
11	Shift Clock	12	Ground
13	Line Clock	14	General Purpose 0
15	MOD	16	Ground
17	FLM (LCD equivalent of VSYNC)	18	Ground
19	Panel Data 0	20	Ground
21	Panel Data 1	22	Panel Data 23
23	Panel Data 2	24	Ground
25	Panel Data 3	26	Panel Data 22
27	Panel Data 4	28	Ground
29	Panel Data 5	30	Panel Data 21
31	Panel Data 6	32	Ground
33	Panel Data 7	34	Panel Data 20
35	Panel Data 8	36	Ground
37	Panel Data 9	38	Panel Data 19
39	Panel Data 10	40	Ground
41	Panel Data 11	42	Panel Data 18
43	Panel Data 12	44	Ground
45	Panel Data 13	46	Panel Data 17
47	Panel Data 14	48	Ground
49	Panel Data 15	50	Panel Data 16

*LCD SECONDARY CONNECTOR FOR 36 BIT PANELS **P24** (2X10 WAY 2MM HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Ground	2	Panel Data 35
3	Panel Data 24	4	Ground
5	Panel Data 25	6	Panel Data 34
7	Ground	8	Panel Data 33
9	Panel Data 26	10	Ground
11	Panel Data 27	12	Panel Data 32
13	Ground	14	Panel Data 31
15	Panel Data 28	16	Ground
17	Panel Data 29	18	Panel Data 30
19	Ground	20	Ground

*DIGITAL VIDEO OPTION **P23** (2X20 WAY 2MM HEADER)*

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Ground	2	VP0
3	Ground	4	VP1
5	Ground	6	VP2
7	Ground	8	VP3
9	Ground	10	VP4
11	Ground	12	VP5
13	Ground	14	VP6
15	Ground	16	VP7
17	Ground	18	VP8
19	Ground	20	VP9
21	Ground	22	VP10
23	Ground	24	VP11
25	Ground	26	VP12
27	Ground	28	VP13
29	Ground	30	VP14
31	Ground	32	VP15
33	Ground	34	HREF
35	Ground	36	VREF
37	Ground	38	VCLK (from Iss 4.0 R261 opt.)
39	Ground	40	Ground

*CD-AUDIO INPUT **P7** (4 WAY BOX SOCKET)*

Pin N°	Signal	Pin N°	Signal
1	CD Audio In Left	2	Audio Ground
3	CD Audio In Right	4	Audio Ground

*AUDIO CONNECTOR **P8** (2X5 WAY 2MM BOX SOCKET)*

Pin N°	Signal	Pin N°	Signal
1	Line In Left	2	Line In Right
3	Audio Ground	4	Audio Ground
5	Microphone In	6	Not Used
7	Audio Ground	8	Audio Ground
9	Line Out Left	10	Line Out Right

*FLOPPY DISK DRIVE CONNECTOR **P12** (2X17 WAY HEADER)*

PIN N°	SIGNAL	PIN N°	SIGNAL
1	Ground	2	Densel
3	Ground	4	Polarisation
5	Ground	6	Rate
7	Ground	8	-Index
9	Ground	10	-Motor 0
11	Ground	12	-Drive select 1
13	Ground	14	-Drive select 0
15	Ground	16	-Motor 1
17	Ground	18	+Direction
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Gate
25	Ground	26	-Track 0
27	Ground	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	+Head Select
33	Ground	34	+Disk Change

*RS485 SERIAL PORT 2 **P14** (2X5 WAY HEADER)*

(DTR sets HDX direction)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	+Rx FDX	2	+Term. 10 K to +5V
3	-Rx FDX	4	No Connect
5	+Tx FDX, +Rx/+Tx HDX	6	No Connect
7	-Tx FDX, -RX/-Tx HDX	8	Polarisation
9	-Term. 10 K to Gnd	10	No Connect

*IRDA CONNECTOR **JP5** (5 WAY HEADER)*

Pin N°	Signal
1	VCC
2	Polarisation
3	RRX
4	Ground
5	RTX

*BATTERY CONNECTOR **P1** (4 WAY HEADER)*

Pin N°	Signal
1	+3.6 Volts DC
2	Polarisation
3	Ground
4	Ground

*FAN POWER CONNECTOR **J19** (2 WAY HEADER)*

Pin N°	Signal
1	Ground
2	+12 Volts DC

*LCD VEE INTERFACE CONNECTOR **JP4** (5 WAY HEADER)*

(Link 3-4 to pass signal to P11-5)

Pin N°	Signal
1	VCC
2	Polarisation
3	Enable VEE
4	Switched VEE (to LCD connector)
5	Ground

*POWER CONNECTOR **J20** (4 WAY)*

Pin N°	Signal
Standard 5.25" Disk Drive Connector	+5 Volts DC
	0 Volts
	0 Volts
	+12 Volts DC (Only required for Ethernet and audio).

*UTILITY CONNECTOR **P16** (2X10 WAY HEADER)*

PIN N°	SIGNAL	PIN N°	SIGNAL
1	Speaker +ve	2	Speaker -ve
3	Reset +ve	4	Reset -ve (Ground)
5	NU	6	NU
7	Keylock +ve	8	Keylock -ve (Ground)
9	Power LED +ve	10	Power LED -ve (Ground)
11	External SMI +ve	12	External SMI -ve (Ground)
13	IDE LED +ve	14	IDE LED -ve
15	+5V limited current	16	0 Volts (Ground)
17	External Battery	18	0 Volts Battery (Ground)
19	Keyboard Data	20	Keyboard Clock

*COAST CACHE CONNECTOR **P3***

This is an industry-standard connector for **C**ache **O**n **A** **St**ick. The COAST connector is a 160-pin socket which is designed to prevent reversed fitting of the cache module.

Please note that each cache module is designed specifically for each chipset i.e. there are cache modules specific to the 430HX Triton chipset. The available options for ATOM cache are 256kbyte asynchronous, 256 or 512KByte of synchronous Pipeline burst, or none.

PINOUT OF ISA, PISA AND PCI CONNECTORS

pin num.	ISA-Bus top layer up row	ISA-Bus bot layer up row	PCI-Bus top layer low row	PCI-Bus bot layer low row	5V PCI Conn side B	5V PCI Conn card side A	universal PCI Conn side B	universal PCI Conn card side A	3.3V PCI Conn side B	3.3V PCI Conn card side A	
1	/IOCHCHK	GND	I2CLK	I2DAT							
2	SD7	RSTDRV	GND	GND							
3	SD6	Vcc	INTB#	INTA#							
4	SD5	IRQ9	INTD#	INTC#							
5	SD4	-5V	Vcc	Vcc							
6	SD3	DRQ2									
7	SD2	-12V	Vcc	V I/O	-12V	TRST#	-12V	TRST#	-12V	TRST#	1
8	SD1	/0WS			TCK	+12V	TCK	+12V	TCK	+12V	2
9	SD0	+12V	PCIRST#	PCICLK2	GND	TMS	GND	TMS	GND	TMS	3
10	IOCHRDY	GND	GNT#0	GND	TDO	TDI	TDO	TDI	TDO	TDI	4
11	AEN	/SMEMW	REQ#0	GNT#1	VCC	VCC	VCC	VCC	VCC	VCC	5
12	SA19	/SMEMR	GND	GND	VCC	INTA#	VCC	INTA#	VCC	INTA#	6
13	SA18	/IOW	PCICLK1	REQ#1	INTB#	INTC#	INTB#	INTC#	INTB#	INTC#	7
14	SA17	/IOR	GND	AD31	INTD#	VCC	INTD#	VCC	INTD#	VCC	8
15	SA16	/DACK3	AD30	AD29	PRSNT1#		PRSNT1#		PRSNT1#		9
16	SA15	DRQ3	CLK	VCC		VCC		V I/O		3.3V	10
17	SA14	/DACK1	GND	GNT#2	PRSNT2#		PRSNT2#		PRSNT2#		11
18	SA13	DRQ1	PCICLK3	REQ#	GND	GND					12
19	SA12	/RFRSH	VCC		GND	GND					13
20	SA11	SYSCLK	AD31	AD30							14
21	SA10	IRQ7	GNT#2	PCICLK4	GND	RST#	GND	RST#	GND	RST#	15
22	SA9	IRQ6	AD28	AD27	CLK	VCC	CLK	V I/O	CLK	3.3V	16
23	SA8	IRQ5	AD26	AD25	GND	GNT#	GND	GNT#	GND	GNT#	17
24	SA7	IRQ4	AD24	CBE#3	REQ#	GND	REQ#	GND	REQ#	GND	18
25	SA6	IRQ3	AD22	AD23	VCC		V I/O		3.3V		19
26	SA5	/DACK2	AD20	AD21	AD31	AD30	AD31	AD30	AD31	AD30	20
27	SA4	T/C	AD18	AD19	AD29	3.3V	AD29	3.3V	AD29	3.3V	21
			PWRGDIN	REQ#3	GND	AD28	GND	AD28	GND	AD28	22
			GND	GNT#3	AD27	AD26	AD27	AD26	AD27	AD26	23
			AD16	AD17	AD25	GND	AD25	GND	AD25	GND	24
					3.3V	AD24	3.3V	AD24	3.3V	AD24	25
					C/BE3#	IDSEL	C/BE3#	IDSEL	C/BE3#	IDSEL	26
					AD23	3.3V	AD23	3.3V	AD23	3.3V	27
					GND	AD22	GND	AD22	GND	AD22	28
					AD21	AD20	AD21	AD20	AD21	AD20	29
					AD19	GND	AD19	GND	AD19	GND	30
					3.3V	AD18	3.3V	AD18	3.3V	AD18	31
					AD17	AD16	AD17	AD16	AD17	AD16	32
					C/BE2#	3.3V	C/BE2#	3.3V	C/BE2#	3.3V	33
					GND	FRAME#	GND	FRAME#	GND	FRAME#	34
					IRDY#	GND	IRDY#	GND	IRDY#	GND	35
					3.3V	TRDY#	3.3V	TRDY#	3.3V	TRDY#	36
					DEVSEL#	GND	DEVSEL#	GND	DEVSEL#	GND	37
					GND	STOP#	GND	STOP#	GND	STOP#	38
					LOCK#	3.3V	LOCK#	3.3V	LOCK#	3.3V	39
					PERR#	SDONE	PERR#	SDONE	PERR#	SDONE	40
					3.3V	SBO#	3.3V	SBO#	3.3V	SBO#	41
					SERR#	GND	SERR#	GND	SERR#	GND	42

28	SA3	BALE			3.3V	PAR	3.3V	PAR	3.3V	PAR	43
			FRAME#	IRDY#	C/BE1#	AD15	C/BE1#	AD15	C/BE1#	AD15	44
29	SA2	Vcc			AD14	3.3V	AD14	3.3V	AD14	3.3V	45
			CBE#2	DEVSEL#	GND	AD13	GND	AD13	GND	AD13	46
30	SA1	OSC			AD12	AD11	AD12	AD11	AD12	AD11	47
			TRDY#	LOCK#	AD10	GND	AD10	GND	AD10	GND	48
31	SA0	GND			GND	AD09	GND	AD09	M66EN	AD09	49
			STOP#	PERR#					GND	GND	50
32									GND	GND	51
					AD08	C/BE0#	AD08	C/BE0#	AD08	C/BE0#	52
33					AD07	3.3V	AD07	3.3V	AD07	3.3V	53
			GND	SERR#	3.3V	AD06	3.3V	AD06	3.3V	AD06	54
34					AD05	AD04	AD05	AD04	AD05	AD04	55
				AD15	AD03	GND	AD03	GND	AD03	GND	56
35	/SBHE	/MCS16			GND	AD02	GND	AD02	GND	AD02	57
			CBE#1	AD14	AD01	AD00	AD01	AD00	AD01	AD00	58
36	LA23	/IOCS16			VCC	VCC	V I/O	V I/O	VCC	VCC	59
			PAR	AD12	ACK64#	REQ64#	ACK64#	REQ64#	ACK64#	REQ64#	60
37	LA22	IRQ10			VCC	VCC	VCC	VCC	VCC	VCC	61
			GND	GND	VCC	VCC	VCC	VCC	VCC	VCC	62
38	LA21	IRQ11									
39	LA20	IRQ12									
			GND	M66EN							
40	LA19	IRQ15									
			AD13	AD10							
41	LA18	IRQ14									
			AD11	AD8							
42	LA17	/DACK0									
			AD9	AD7							
43	/MEMR	DRQ0									
			CBE#0	AD5							
44	/MEMW	/DACK5									
			AD6	AD3							
45	S D8	DRQ5									
			AD4	AD1							
46	SD9	/DACK6									
			AD2	AD0							
47	SD10	DRQ6									
48	SD11	/DACK7									
			Vcc	V I/O							
49	SD12	DRQ7									
			Vcc	Vcc							
50	SD13	Vcc									
			GND	GND							
51	SD14	/MASTER									
			GND	GND							
52	SD15	GND									

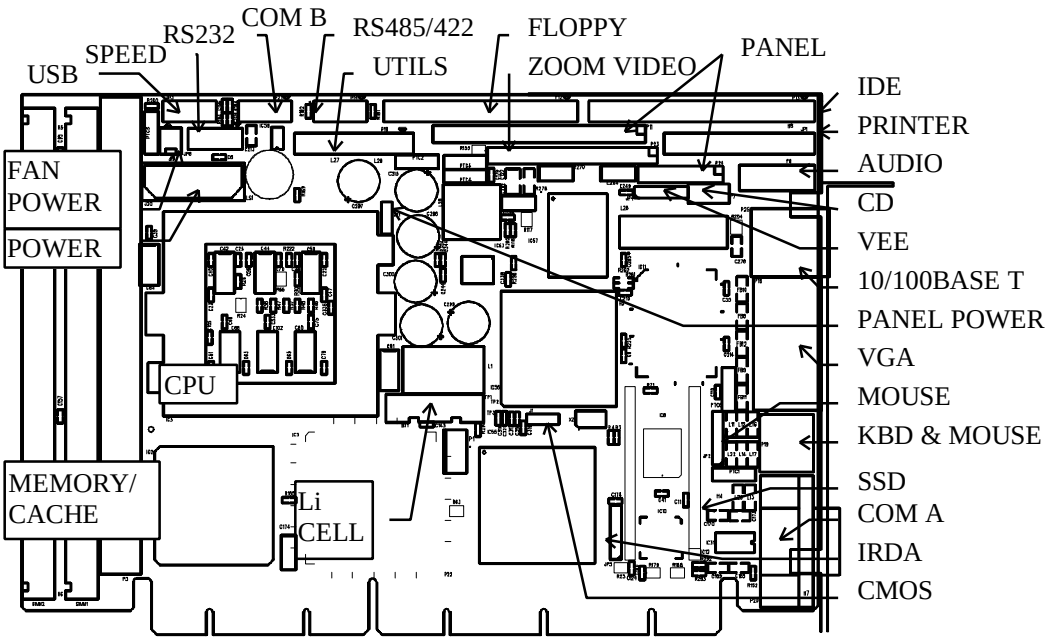
ERROR MESSAGES

Error Beep Codes

The BIOS performs a **P**ower **O**n **S**elf **T**est (POST) after a reset or reboot. If errors occur during the POST, the microprocessor indicates the status of the test by writing codes to the I/O port at address 80 Hex.

Some of the fatal errors produce audible codes which indicate the source of the problem. For a list of these refer to BIOSERR.PDF.

BOARD LAYOUT



All open header pin 1 towards metal bracket =>. Square pad identifies pin 1.
PISA and ISA board versions identical except for edge fingers.

solid state disk (SSD) Orientation

Locate device as shown into above diagram.